Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method. comprising: for

determining a plurality of filter coefficients for a digital filter for a Universal Mobile Telecommunication System (UMTS), in which the filter coefficients are predetermined and modified in a filter design program, comprising the steps of the determining including:

dividing the predetermined initial filter coefficients (θ_{\downarrow}) by a same scaling factor (s), to result in a plurality of scaled filter coefficients (θ_{\downarrow});

quantizing the scaled filter coefficients (β_ν)—so that only a certain maximum number (n) of "1" bits are counted from a most significant bit onwards: and in that

determining a respective quantization error of each quantized scaled filter coefficient is determined relative to a respective one of the predetermined initial filter coefficient coefficients; and

repeatedly modifying for a predetermined-number of times the scaling factor (s) of a respective and determining which scaling factor (s₀) being set results in which the a quantization error becomes a predetermined having minimal error value, and in that

implementing in the filter the filter coefficients (β_*) having resulting in the minimal error are implemented in the filtervalue.

- 2. (Currently Amended) A method as claimed in claim 1, eharacterized in that wherein the number (n) comprises one of four, three, or two.
- 3. (Currently Amended) A method as claimed in claim 1, wherein characterized in that if again a "1" bit follows the last "1" bit, a rounding is effected from the last bit onwards.

4. (Currently Amended) A digital filter for a Universal Mobile Telecommunication System (UMTS), in which the digital filter coefficients are processed with the signal, comprising

means for dividing a plurality of binary filter coefficients (b_w) -by a scaling factor (s_0) -to result in a plurality of scaled filter coefficients (β_w) -;

means for quantizing the <u>scaled</u> filter coefficients (β_v)-so that they do not exceed a <u>predetermined-selected</u> number (n) of "1" bits from a most significant bit onwards, in that; and

adder stages ADD(3)-for processing the scaled and quantized filter coefficients (β_4) -with the an input signal.

- 5. (Currently Amended) The digital filter as claimed in claim 4, comprising a final stage (4) for processing an output signal by a factor (s₀) reciprocal to the scaling factor.
- 6. (Currently Amended) A digital filter as claimed in claim 4, characterized in that wherein each adder stage (3) comprises n-1 adders (9, 10, 11) and a means for multiplying an input by 2^j by shifting the input by i (5, 6, 7, 8), the input being a respective one of the scaled and quantized filter coefficients.
- 7. (Currently Amended) A digital filter as claimed in claim 4, characterized in that in wherein the adder stages (3) and a number n include first and second adder stages respectively including:

respective numbers of a multiplying means for multiplying an input by 2^J by shifting the input by i (5, 6, 7, 8) is , wherein the respective numbers of multiplying means are different; and the number

respective numbers of adders (9, 10, 11) is accordingly coupled to the respective multiplying means, wherein the respective numbers of adders are different.

- 8. (Currently Amended) A digital filter as claimed in claim 7, characterized in that individual wherein the adder stages (3) have include a third adder stage having only a single multiplying means (5) for multiplying an input by 2ⁱ by shifting the input by i.
- 9. (Currently Amended) A digital filter as claimed in claim 4, characterized in that the mean wherein each adder stage comprises n-1 adders and means for multiplying an input by 2^j by shifting the input by i, the input being a respective one of the scaled and quantized filter coefficients, wherein each of the means for multiplying (5, 6, 7, 8) an the input by 2^j by shifting the input by i is formed by connections of its inputs and outputs of a multiplier stage.
- 10. (Currently Amended) A digital filter as claimed in claim 4, characterized in that the wherein each adder stage (3)-comprises:

n-1 adders;

multiplying means for multiplying an input by 2ⁱ by shifting the input by i, the input being a respective one of the scaled and quantized filter coefficients; and

a programmable selector (12) which in accordance with its programming connects the <u>multiplying</u> means for multiplying an input by 2^i by shifting the input by i (5, 6, 7, 8) with the adders (9, 11).

11. (Currently Amended) The method according to claim 1, further comprising

multiplying (5, 6, 7, 8) an input by 2^j by shifting the input by i with and summing shifted values using a plurality of adders (9, 11).

12. (Currently Amended) The method according to claim 1, further comprising:

multiplying an input by 2^j by shifting the input by i (5, 6, 7, 8), which is using a multiplier formed by connections of its inputs and outputs.

- 13. (Currently Amended) The method according to claim 11, wherein adders stage (3) comprises the multiplying is performed using a plurality of multipliers, the method further comprising selectively connecting the multipliers with the adders using a programmable selector (12) which in accordance with its a programming connects the shifted input with the adders (9, 11).
 - 14. (New) A method, comprising:

producing a plurality of scaled filter coefficients by dividing initial filter coefficients by a scaling factor;

quantizing the scaled filter coefficients so that only a certain maximum number (n) of "1" bits are counted from a most significant bit onwards;

determining respective quantization errors of the quantized scaled filter coefficients relative to the initial filter coefficients, respectively; and

modifying the scaling factor and determining which scaling factor results in a quantization error having minimal error value, and

implementing in the filter the filter coefficients resulting in the minimal error value.

- 15. (New) A method as claimed in claim 14, wherein the number (n) comprises one of four, three, or two.
- 16 (New) A method as claimed in claim 14, wherein if again a "1" bit follows the last "1" bit, a rounding is effected from the last bit onwards.
- 17. (New) The method according to claim 14, further comprising:
 multiplying an input by 2^j by shifting the input by i using a multiplier formed by
 connections of inputs and outputs.

Application No. 10/532,903 Reply to Notice of Allowance dated October 10, 2008

- 18. (New) The method according to claim 14, further comprising multiplying an input by 2^j by shifting the input by i and summing shifted values using a plurality of adders.
- 19. (New) The method according to claim 18, wherein the multiplying is performed using a plurality of multipliers, the method further comprising selectively connecting the multipliers with the adders using a programmable selector in accordance with a programming.